OHMIC CONTACT TO SEMICONDUCTOR

REFERENCE TO RELATED APPLICATIONS

The current application is a divisional of U.S. patent application Ser. No. 13/775,038, which was filed on 22 Feb. 2013, and which claims the benefit of U.S. Provisional Application No. 61/602,155, which was filed on 23 Feb. 2012, both of which are hereby incorporated by reference.

TECHNICAL FIELD

The disclosure relates generally to contacts to semiconductors, and more particularly, to an ohmic contact to a semiconductor, such as a nitride-based semiconductor.

BACKGROUND ART

A challenge in developing high power III-V material-based semiconductor devices, such as light emitting diodes (LEDs), laser diodes (LDs), bipolar junction transistors (BJTs), and heterojunction bipolar transistors (HBTs), is the development of an ohmic contact that has both a low specific resistance and a high current carrying capability. For example, the challenge to manufacture a low resistance ohmic contact to n-type material is particularly important for deep ultraviolet LEDs made from group III-nitride materials, such as Aluminum Gallium Nitride (AlGaN) or Aluminum Gallium Indium Nitride (AlGaInN), which include a high molar fraction of aluminum.

To achieve a low n-type contact resistance in a nitride-based device, several contact metals and a relatively high annealing temperature are generally used. To this extent, Al can be used as a contact metal because of its relatively low melting point of approximately 660 degrees Celsius. Furthermore, Titanium (Ti) or Chromium (Cr) can be used as the first layer of the contact due to their low metal work function to nitrides. Specific examples include Ti/Al/Ti/Gold (Au) or Ti/Al/Nickel (Ni)/Au, with thicknesses from five nanometers to five microns and which are annealed at 400 degrees Celsius or higher temperatures. Another approach reverses the order of the Ti and Al, and forms an Al/Ti-based contact to an n-type GaN semiconductor, which includes Al/Ti/Platinum (Pt)/Au and which is annealed at temperatures between 400 and 600 degrees Celsius. Still other approaches form a Cr/Al-based contact to an n-type GaN semiconductor, which include various metal configurations, such as Cr/Al/Cr/Au, Cr/Al/Pt/Au, Cr/Al/Pd/Au, Cr/Al/Ti/Au, Cr/Al/Cobalt (Co)/Au, and Cr/Al/Ni/Au.

Contact reliability also can be a problem. For example, to date, Ti/Al-based n-type contacts for ultraviolet LEDs emitting 265 nanometer and shorter wavelengths have not been shown to be very reliable.

Some approaches have improved an ohmic contact through re-growing semiconductor layers after performing the etching process. For example, in one approach, a non-alloyed contact is formed through a process of re-growing semiconductor layers. The process includes: (1) growing semiconductor layers on a substrate such as sapphire; (2) disposing a regrowth mask above the top semiconductor layer, where the regrowth mask material (e.g., silicon nitride or silicon dioxide) is chosen, deposited, and selectively removed (e.g., through the use of a photoresist) so that is can function as a passivation layer on the semiconductor surface; (3) etching the semiconductor layers with an acceptable depth being approximately five to one thousand nanometers past the surface of the top semiconductor layer; (4) growing

structures in the etched regions; and (5) optionally applying photolithography to define a gate region for devices that include gates.

FIGS. **1**A-**1**C show typical ohmic contacts **2**A-**2**C, respectively, formed using reactive ion etching (RIE) and re-growth processes according to the prior art. In each case, RIE of a semiconductor layer **4**A-**4**C is employed prior to re-growth. Re-growth is carried through with subsequent deposition of an ohmic metal **6**A-**6**C. In FIG. **1**A, the ohmic contact **2**A includes a regrown surface state compensating layer on the RIE damaged layer **4**A. In FIG. **1**B, the ohmic contact **2**B includes a regrown surface state compensating layer and a delta doping layer. In FIG. **1**C, the ohmic contact **2**C includes a regrown surface state compensating layer and a layer for low specific ohmic contact resistance. As illustrated in FIGS. **1**A-**1**C, the regrown technique can be used in conjunction with other features, such as delta-doping as shown in FIG. **1**B. The delta-doping has significance for high speed devices, such as heterostructure field-effect transistors, which employ the delta-doping technique to achieve a high carrier density, and large breakdown voltage of the gate. In addition, the regrowth technique can be used together with contacts that include a rough morphology as shown in FIG. **1**C, as well as contacts that are annealed with regrowth regions and have protrusions into regrowth region. While the quality of each of the contacts **2**A-**2**C is significantly improved by re-growing as compared to direct deposition of the ohmic metal **6**A-**6**C, each process has a large number of defects in the RIE etched region **4**A-**4**C, which reduces the quality of the ohmic contact **2**A-**2**C and decreases an overall lifetime of the corresponding device including the ohmic contact **2**A-**2**C.

Another regrowth approach is specifically designed to regrow group III nitride semiconductor layers. The process includes: (1) growing a semiconductor body on a substrate including semiconductor layers with an unintentionally doped (UID) gallium nitride (GaN) layer overlying the semiconductor layers and a UID aluminum gallium nitride (UID-AlGaN) layer overlying GaN semiconductor layers; (2) depositing and patterning an insulating film; and (3) re-growing an n+ GaN layer at regions of the surface of the UID-AlGaN not covered with insulating film without etching the surface of the UID-AlGaN semiconductor.

SUMMARY OF THE INVENTION

Aspects of the invention provide a solution for forming an ohmic contact to a semiconductor layer. A masking material is applied to a set of contact regions on the surface of the semiconductor layer. Subsequently, one or more layers of a device heterostructure are formed on the non-masked region (s) of the semiconductor layer. The ohmic contact can be formed after the one or more layers of the device heterostructure are formed. The ohmic contact formation can be performed at a processing temperature lower than a temperature range within which a quality of a material forming any semiconductor layer in the device heterostructure is damaged.

A first aspect of the invention provides a method comprising: forming a device heterostructure including an ohmic contact to a semiconductor layer in a set of semiconductor layers of the device heterostructure without etching the semiconductor layer, wherein the forming includes: applying a masking material on a set of contact regions corresponding to the ohmic contact on a surface of the semiconductor layer; forming a protruded region over a set of unmasked regions of the surface of the semiconductor layer